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(54) **SEMICONDUCTOR MEMORY**

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor memory in which the write-in speed can be increased and the chip size can be reduced though the memory is provided with a write-in data mask and has a multi-bit constitution corresponding to plural word constitutions.

SOLUTION: A write-in circuit (B) 103 can be constituted of a logic circuit of two inputs, output signals WDB and NWBD from a write-in circuit (A) 102 being each input signal of the write-in circuit (B) 103 are made complementary signal based on polarity of write-in data DI in a non-mask bit and a selection bit, and they are made mutually the same polarity independently of a polarity of the write-in data DI in a mask bit, a non-mask bit, and a non- selection bit.